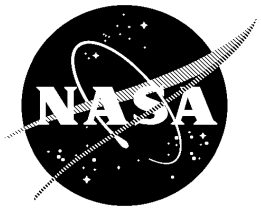
EO-1 ICD-067
Baseline
March 18, 1999

Earth Orbiter-1 (EO-1) WARP FLIGHT HARDWARE

S-Band, WARP to C&DH Subsystem Interface Control Document



National Aeronautics and Space Administration

Goddard Space Flight Center
Greenbelt, Maryland

EO-1 ICD-067
Baseline
March 18, 1999

Earth Orbiter-1 (EO-1) S-Band WARP to C&DH Subsystem

Interface Control Document

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1. TBD List

Issue	Section Number	Resolution Date	Comment

2. Change Information Page

List of Effective Pages	
Page Number	**Issue**
Title page	Baseline
ii through iv	Baseline
1-1 through	Baseline
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Revision	Description	Date	Approval
–	Initial Release		3/18/99

1 OVERVIEW

1.2 Scope

This document describes the S-Band interface from the Wideband Advanced Recorder Processor (WARP) via the ACDS subsystem to the Comm RSN.

1.2 Supporting Documents

Title	Source	Date
WARP to Ground ICD, Rev. D, by Tim Leath & Jack Shih	GSFC	1998
Spacecraft 1773 Data Bus ICD, by Tim Leath	GSFC	1997
WARP Integration & Test Specifications, by Wes Powell	GSFC	1997
Comm RSN Interface Description Document	Litton	1998

1.3 Requirements

The Medium Speed Serial Port (MSSP) interface is required to provide a continuous downlink at a rate of 2 Mbps via the EO-1 C&DH to the Comm RSN. The MSSP will be used to transport housekeeping frames and raw science data stored in the EO-1 WARP SSR bulk memory to the Comm RSN and eventually to the ground for processing. The data transferred between the EO-1 WARP SSR and the Comm RSN will be based on the CCSDS 701 AOS packet structure. (see WARP to Ground ICD)

1.4 Interface Overview

Figure 1 illustrates the data flow from the WARP via the C&DH to the S-Band Comm RSN.

1.4.1 WARP Interface Overview

The design is based on the use of two separate (32K x 16) MSSP packet buffer memories, A and B, set up in a “ping-pong” arrangement. During data transmission, the MSSP unloads one memory (say A) while the WARP M5 reloads the other (B). When done unloading A, the MSSP immediately starts unloading B (assuming it has been reloaded in time) and signals to the WARP M5 that A is empty and needs reloading.

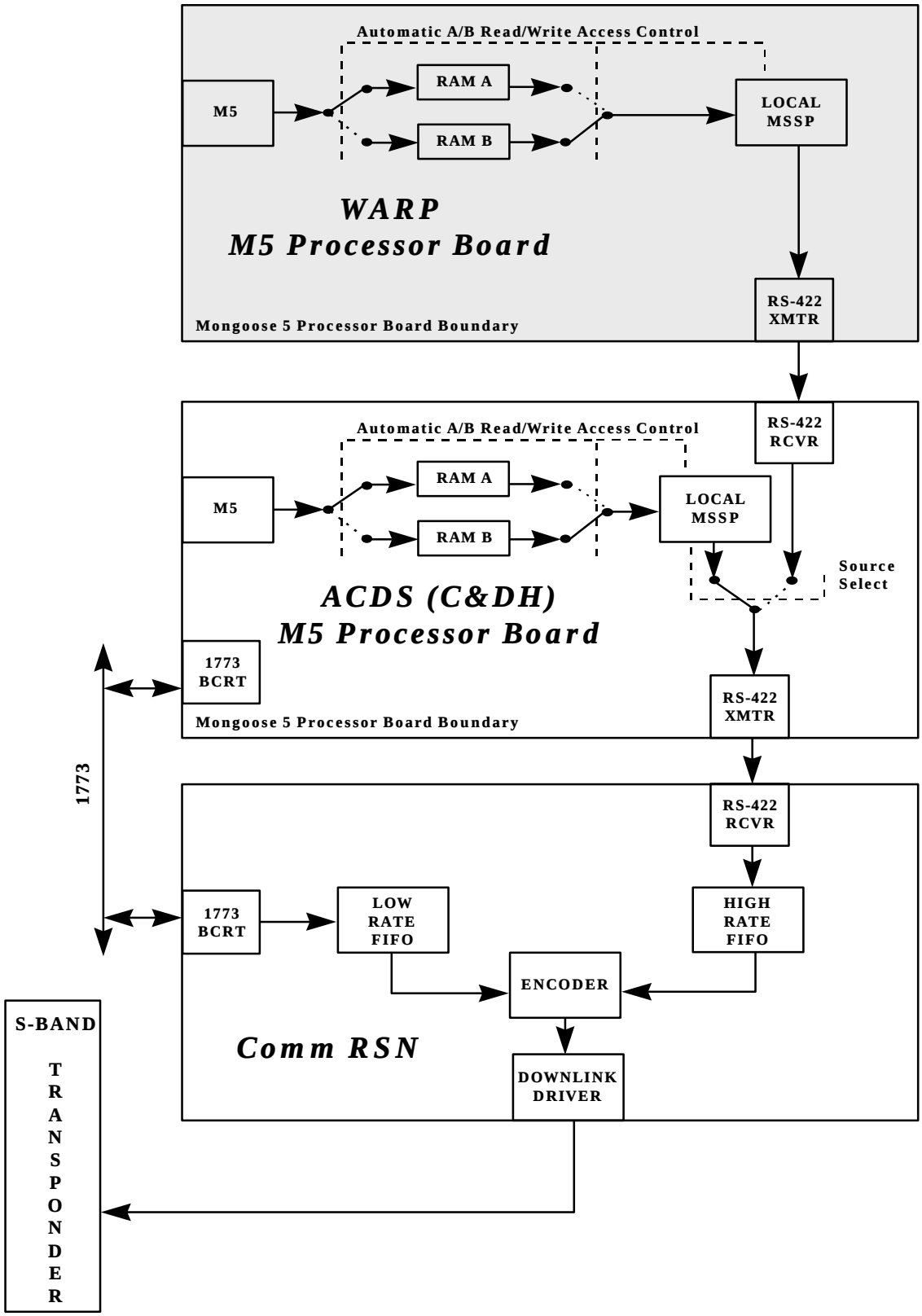

Automatic A/B Read/Write Access Control
M5
RAM A
RAM B
LOCAL MSSP
WARP
M5 Processor Board
RS-422 XMTR
Mongoose 5 Processor Board Boundary
RS-422 RCVR
Automatic A/B Read/Write Access Control
M5
RAM A
RAM B
LOCAL MSSP
Source Select
ACDS (C&DH)
M5 Processor Board
1773 BCRT
RS-422 XMTR
Mongoose 5 Processor Board Boundary
1773
RS-422 RCVR
1773 BCRT
LOW RATE FIFO
HIGH RATE FIFO
ENCODER
Comm RSN
DOWNLINK DRIVER
S-BAND TRANSPONDER

Figure 1 - Data Flow Diagram

The left side of Figure 1 of the WARP M5 Processor Board depicts the alternating paths for M5 or MSSP access to RAMs A and B. The leftmost "switch" in the figure shows the M5 connected for read/write access to reload RAM A, while the next switch connects the local MSSP for read access unloading of RAM B. When RAM B empties out, both switches will automatically and simultaneously flip to the other position. The right side of Figure 1 of the ACDS (C&DH) M5 Processor Board shows the switches for source and destination selection, which can be controlled by jumpers or software.

The MSSP has two operating modes. The test mode, called Local Setup/Test (LST) allows the WARP M5 local read/write access to the MSSP RAMs and registers. There is no serial output in this mode. The operating mode, called Automatic Transmit/Reload (ATR), allows the WARP M5 to read the control and status registers but can only read/write access one of the two RAMs. The MSSP has read-only access to the RAM for serial data transmission.

The WARP M5 software issues a START command to go from LST mode to ATR mode, and issues a STOP command to go from ATR mode back to LST mode.

1.4.2 Comm RSN Overview

The Comm RSN is an essential component in the communications link between the ground system and the EO-1 WARP. As such, the Comm RSN shall receive CCSDS (Consultative Committee for Space Data Systems) uplink codeblocks from the transponder and pass them to the C&DH. The Comm RSN shall also receive CCSDS downlink frames from the WARP, format and encode them, and send them to the transponder.

1.5 Interface Layers Description

This document will use a modified Open Systems Interconnection (OSI) standard model, which describes an interface between two systems. Each system performs functions, which can be described as a series of layers. Each system has the same number of layers, and the equivalent layers for each system communicate via an established protocol, which is transparent to the protocols at other layers. Each system passes data from its upper layers to the lower layers via a service provided by the next lower layer. OSI uses seven layers to describe an interface but for the purpose of this document, three layers will be utilized: the Physical Layer (Layer 1), the Data Link

Layer (Layer 2), and the Application Layer (Layer 3). The first two layers are identical to those of the OSI standard, and the third layer corresponds to the upper software-oriented functions of the interface.

2 PHYSICAL LAYER

2.2 Physical Layer Function

The Physical Layer consists of two parts: the physical layer medium (the cabling and connectors etc. that make up the physical connection between the two systems) and the physical layer protocol that defines the lowest level of formatting (bit-level) of the data.

2.3 Mechanical Interface

2.3.1 Fasteners and Clamping

Jack screws on the cable are connected to jack posts on the connector.

2.3.2 Connector Keying

D-Connectors are used on each side which prevents from putting them backwards.

2.4 Cable Type

For data lines utilizing RS-422, twisted-shielded pair cables are required.

2.4.1 Maximum Cable Length

Cable length can reach as high as 30 feet.

2.4.2 Wire Gauge

24-gauge wire will be used.

2.4.3 Shield Connections

Shield connections are terminated to the back shell of each end of the harness.

2.5 Connector Type

44-pin D-Connector is utilized (Part # 311P407-3S-B-12) on both the ACDS and the WARP.

2.5.1 Connector Pin-out

The following is the connector pin-out:

From WARP M5	Pin	To ACDS M5	Pin
XPDRA_DAT+	16	SCI_DAT+	24
XPDRA_DAT-	1	SCI_DAT-	9
XPDRA_CLK+	17	SCI_CLK+	25
XPDRA_CLK-	2	SCI_CLK-	10
XPDRA_RTS+	18	SCI_RTS+	26
XPDRA_RTS-	3	SCI_RTS-	11
To WARP M5	**Pin**	**From ACDS M5**	**Pin**
XPDRA_CTS+	19	SCI_CTS+	27
XPDRA_CTS-	4	SCI_CTS-	12

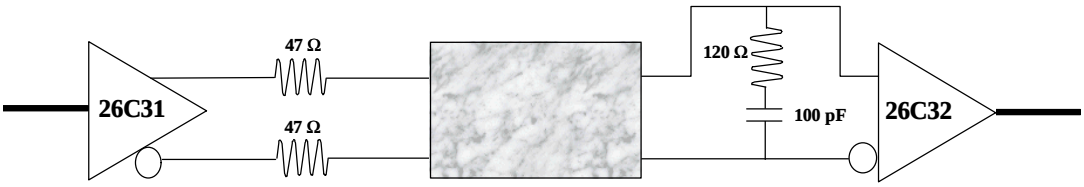
2.6 Bit Level Timing

The MSSP will support instantaneous serial data bit rate to the Comm RSN of 2 Mbps. The bit clock (50% ± 10% duty cycle) will be derived from a 16 MHz crystal oscillator, with data valid during the rising edge of the bit clock. The rise and fall times from the RS-422 receivers are 2 nsecs minimum and 12 nsecs maximum. The rise and fall times from the RS-422 drivers are 1 nsec minimum and 10 nsecs maximum. Serial data out from the MSSP is Most Significant Bit (MSB) first, with 16 serial bit times between successive parallel loads.

2.7 Signal Levels

The output voltages from the RS-422 receivers are >= 3.8V for V_{OH} (High Level Output Voltage) and <= 0.3V for V_{OL} (Low Level Output Voltage). The output voltages from the RS-422 drivers are >= 2.5V for V_{OH} and <= 0.5V for V_{OL}.

2.8 Signal Grounding and Isolation



This design illustrates the proper termination for RS-422 signals. The gray box represents the cable connection from connector A to connector B.

2.9 Handling Procedures

2.9.1 ESD Precautions

The RS-422 signals are generated from HS-26C31RH ICs (Radiation Hardened Quad Differential Line Drivers) and

received from HS-26C32RH ICs (Radiation Hardened Quad Differential Line Receivers). These devices are sensitive to electrostatic discharge. Users should follow proper IC handling procedures.

2.9.2 Connector Installation and Removal

Before connector installation, verify for pin damage and perform safe-to-mate procedures. Also, it is important to always log in the mate.

2.9.3 Maximum Number of Mating and Demating

The maximum number of Mating and Demating is 20.

2.10 EMC/EMI

Electronic components shall be subjected to electromagnetic compatibility (EMC) testing to ensure that they will neither be a source of electromagnetic interference (EMI) when integrated with other components. Testing shall be performed in accordance with the procedures outlined by the EO-1 WARP Integration and Test Specifications.

3 DATA LINK LAYER

3.2 Data Link Layer Function

The main task of the Data Link Layer is to define the basic data units, usually called frames, which are present on the interface and ensures that they are transmitted free of errors from the source to the destination. The frames are created by adding headers and/or trailers to the data at the source, which are recognized by the Data Link Layer service in the receiver. These frames can serve as sync patterns and also as the extra bits required for frame detection and correction. The other principal function of this layer is flow control: managing the volume of data from source to destination so as to prevent overflow and underflow of the buffers on either end. Both flow and error control require acknowledgment from receiver to source, and this acknowledgment scheme is defined at this layer.

3.3 Data Unit Definition

Serial data transfers from the MSSP will be done in blocks (frames), nominally with 1104 bytes (552 half-words) per block (refer to Figure 2). The first half-word (16-bit data word) of a block must be 0x1ACF. The second half-word of a block must be 0xFC1D. These four bytes make up the sync marker that signals the start of CCSDS VCDU transfer frame. The 552nd half-word of a block should be 0x0000, which the Comm RSN will overwrite with a CRC checksum. The middle 549 half-words (1098 bytes) can be any kind of user-defined data. The maximum block size that can be handled by the Comm RSN is 1024 half-words (2048 bytes). The maximum number of blocks that can be stored in either of the (32K x 16) buffer memories is 32. For the purposes of EO-1, the user-defined data field will be in the form of CCSDS packets. The packet will consist of a VCDU Primary Header, VCDU Insert Zone, M_PDU Header, M_PDU Packet Data Zone, Data Zone and a VCDU Trailer (refer to Figure 3).

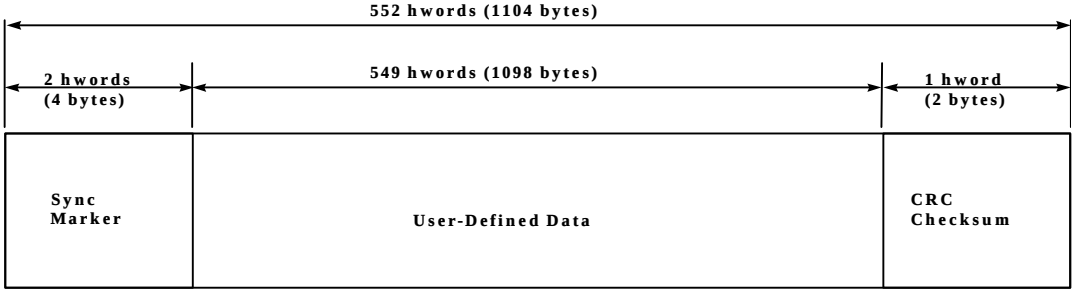


Figure 2 - MSSP Transfer Frame

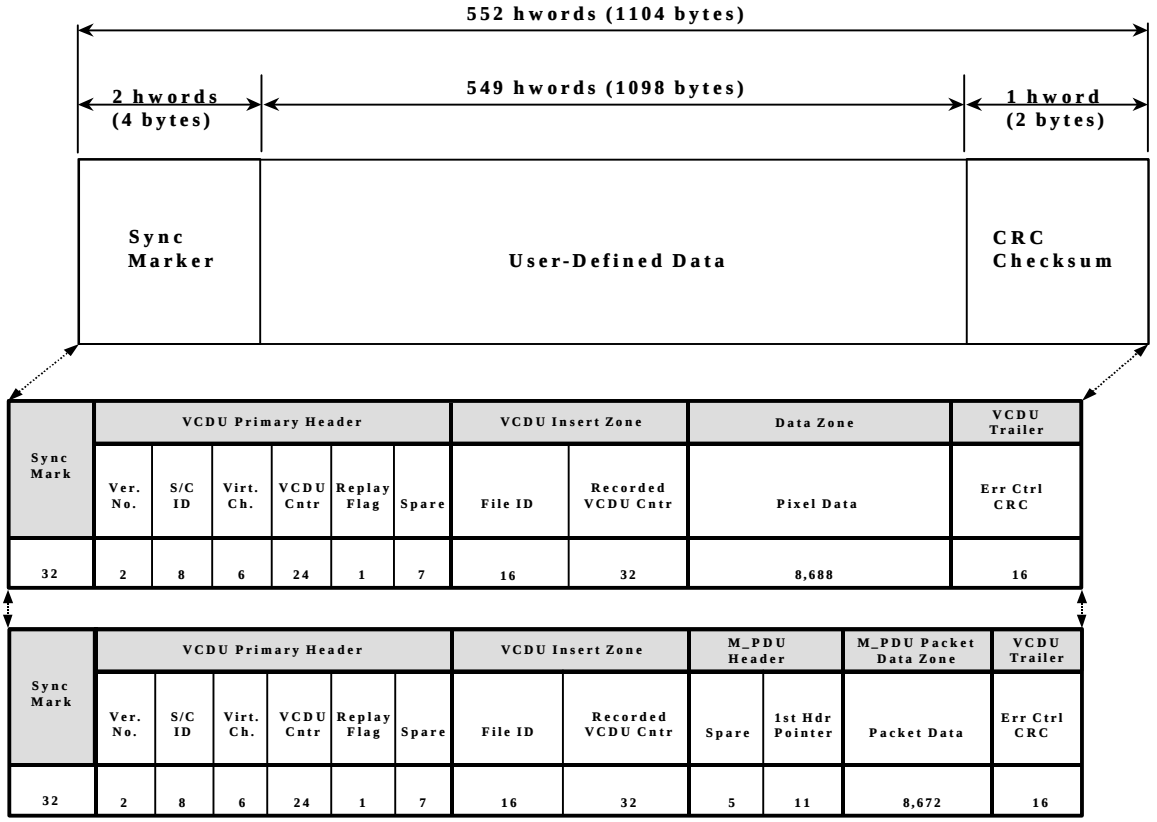


Figure 3 - EO-1 CADU relative to MSSP Transfer Frame (Science Data, Housekeeping Data)

3.4 Flow Control Handshaking between MSSP and Comm RSN

Flow control handshaking will automatically be done by MSSP hardware on a block-by-block basis. The top part of Figure 4 flow diagram shows the block transfer handshake process. Prior to the transmission of any block, the Request To Send (RTS signal from MSSP to Comm RSN) and Clear To Send (CTS signal from Comm RSN to MSSP) will initially be deasserted. With a block ready for transmission, the MSSP asserts RTS high to signal “data ready”. The MSSP then waits until Comm RSN asserts CTS high to signal “go ahead”. The MSSP automatically clocks out a full block to the Comm RSN and then must deassert RTS to signal “block transfer complete”. The Comm RSN then deasserts CTS to signal “not ready for next block”. RTS and CTS are now both deasserted, and the process repeats for each subsequent block of data. The waveform diagram is provided by Figure 5 and Table 1 provides the high rate telemetry timing. If the WARP detects CTS = 0 before it has completed transmitting a frame, the WARP shall retransmit that frame. If the Comm RSN detects RTS = 0 before the frame has been completely received, either a High Rate FIFO overflow or a High Rate Sync Error

will occur. In either case, the Comm RSN downlink must then be reset. Please refer to Section 5.4 for more detailed information on the MSSP operational timeline.

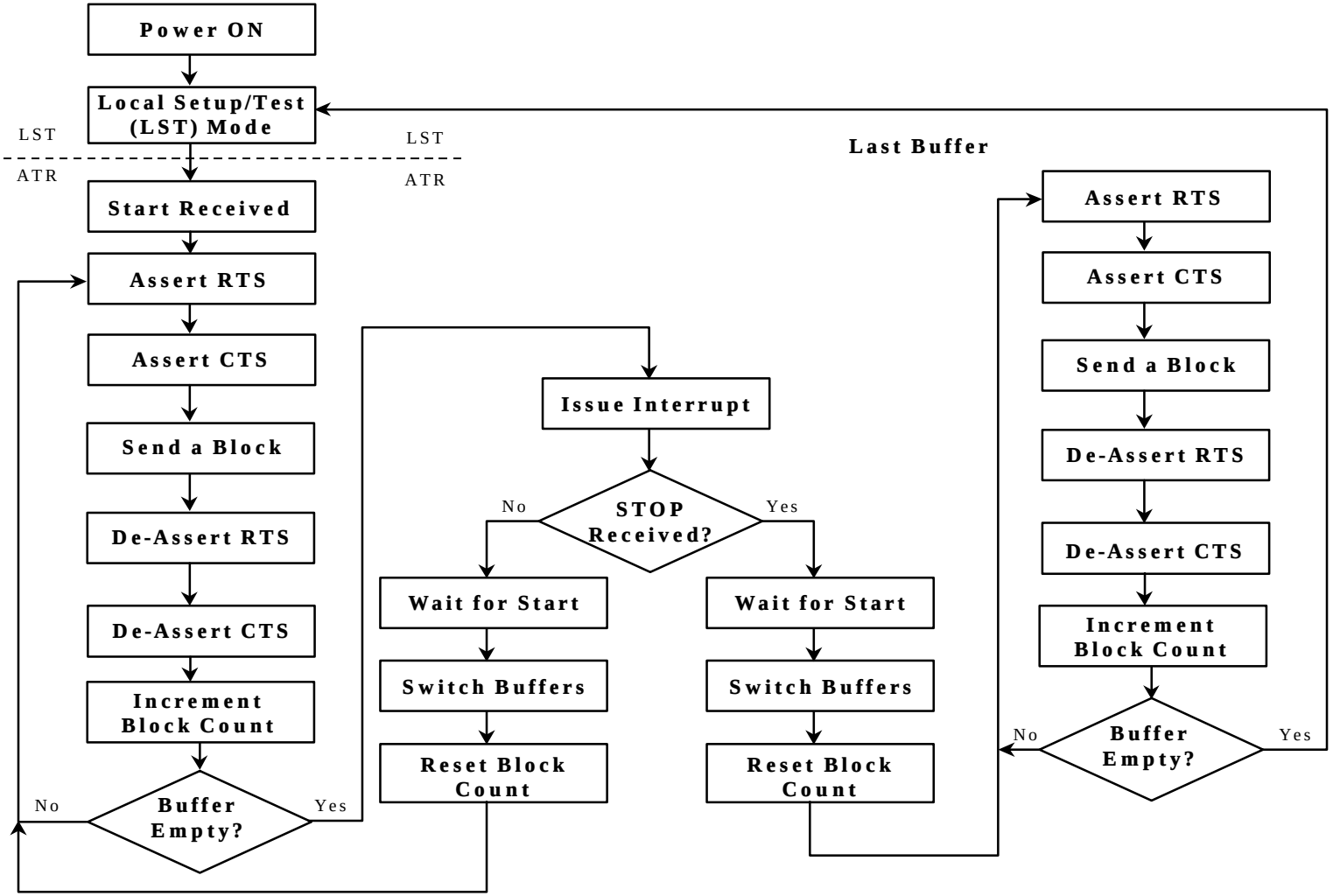
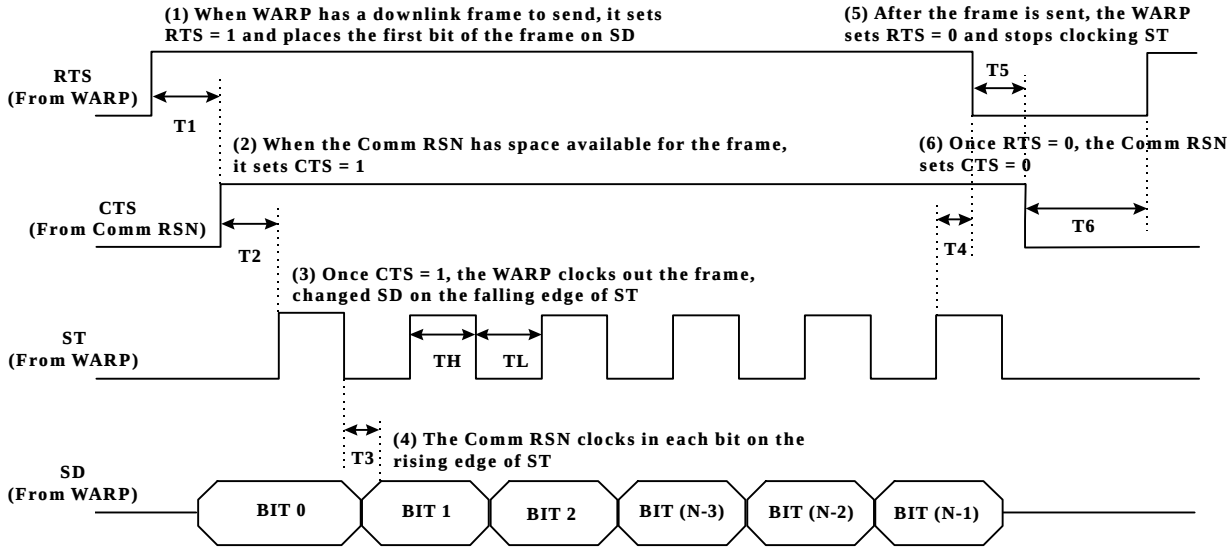


Figure 4-1 - MSSP Flow Chart



RTS = Request to Send
CTS = Clear to Send
ST = Send Timing
SD = Send Data

Figure 4-2 - High Rate Protocol

Table 1 - High Rate Telemetry Timing

Time	Description	Min	Max
T1	From RTS (H) to CTS (H)	45 ns	Infinite
T2	From CTS (H) to ST (H)	0	62.5 ns
T3	From ST (L) to SD stable	0	30 ns
T4	From Last ST (H) to RTS (L)	62.5 ns	Infinite
T5	From RTS (L) to CTS (L)	0	45 ns
T6	From CTS (L) to RTS (H)	125 ns	Infinite
TL	From ST (L) to ST (H)	62.5 ns (50%±10% Duty Cycle)	Infinite
TH	From ST (H) to ST (L)	62.5 ns (50%±10% Duty Cycle)	Infinite

H = Rising edge
L = Falling edge

4 APPLICATION LAYER

This section is contained in the WARP to Ground ICD.

5 IMPLEMENTATION NOTES

This section provides more details on the Medium Speed Serial Port.

5.2 WARP M5 Data Accesses to MSSP

To cut down on the number of required parts and FPGA I/O pins, simplify the logic design, and not have to worry about compiler/assembler support for certain types of LR33300 paired half-word read/write cycles, the WARP M5 data accesses to MSSP memory and registers will be 16 bits wide. The easiest implementation will probably be to do normal 32-bit LOAD/STORE, operations on word address boundaries where only the 16 Least Significant Bits (LSBs) are used. On a word write from the WARP M5 to the MSSP memory, the least significant half-word would be written and the most significant half-word would be ignored (don't care). On a word read from the MSSP by the WARP M5, the least significant half-word would be read and the most significant half-word would probably be 0xFFFF (from tri-stated bus with pull-ups).

Each of the two (32K x 16) buffer memories can hold 32 blocks if each block is the maximum possible size (2048 bytes). In this case, each block would start at a 1 Kword address boundary and the buffer memory would be completely full. In order to simplify the MSSP design, each block will always start at a 1 Kword address boundary even if it is 552 half-words in size and not the maximum 1024 half-word size. Figure 6 shows the start addresses for data block storage in the buffer memories. The first block is loaded starting at word address 0xBE30.0000. The second block is loaded starting at 0xBE30.1000, etc. The shaded areas correspond to unused areas of memory if the block size is 552 half-words instead of the maximum size of 1024 half-words.

If the telemetry data is stored as 32-bit words in WARP M5 SSR DRAM, then the WARP M5 would fetch a 32-bit word from DRAM, write the word to an MSSP word address (16 LSBs = least significant half-word first), shift the same word right by 16 bits, and then write the result to the next MSSP word address (16 MSBs = most significant half-word second).

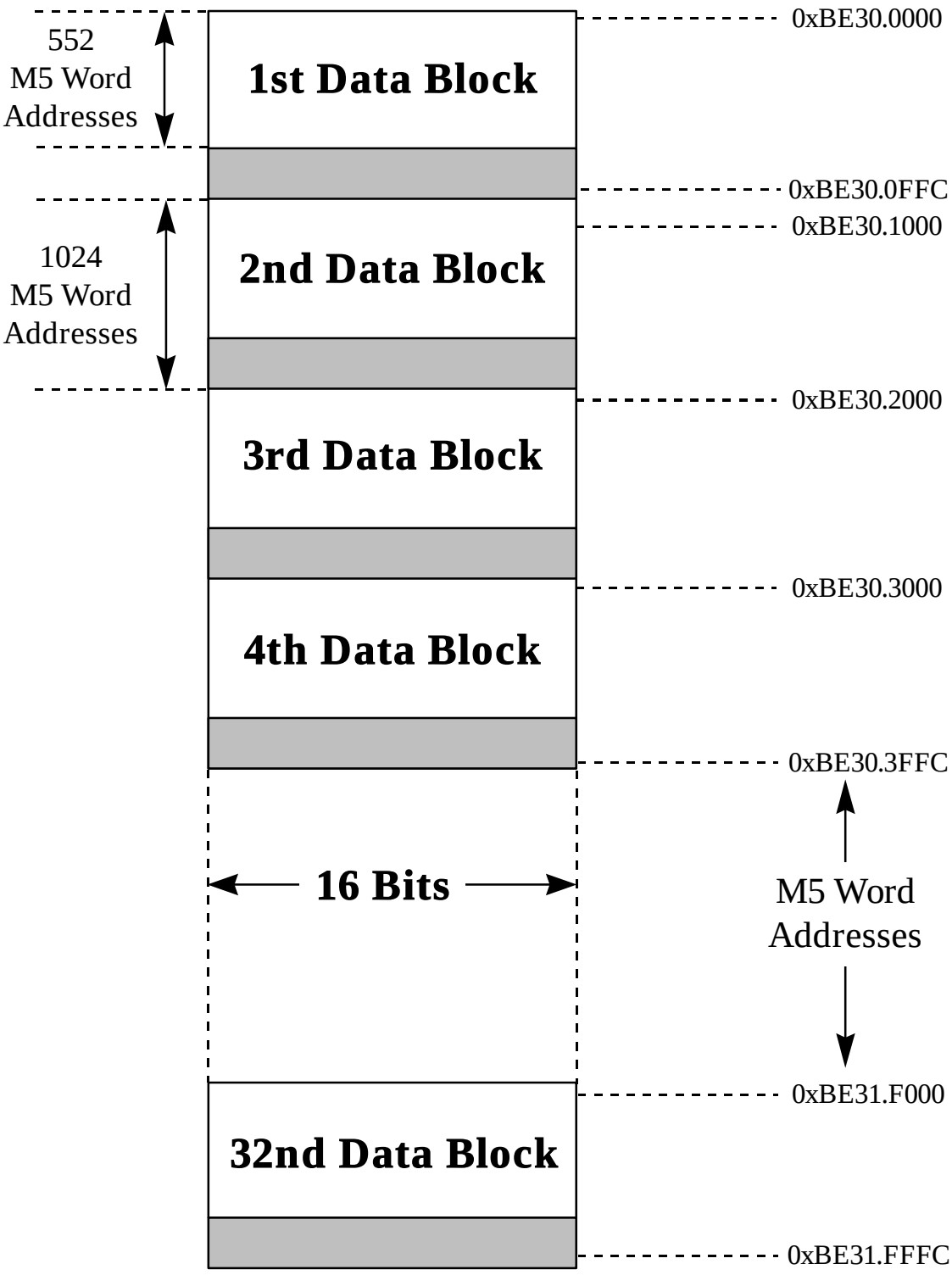

552
M5 Word
Addresses
1st Data Block
0xBE30.0000
0xBE30.0FFC
1024
M5 Word
Addresses
2nd Data Block
0xBE30.1000
0xBE30.2000
3rd Data Block
0xBE30.3000
4th Data Block
0xBE30.3FFC
16 Bits
M5 Word
Addresses
0xBE31.F000
32nd Data Block
0xBE31.FFFC

Figure 5-1 - MSSP Buffer Memory Block Start Addresses

5.3 Buffer Reload Handshaking between MSSP and WARP M5 Software

When transmission has started, the MSSP unloads RAM B buffer a block at a time. When the B buffer is empty, the MSSP automatically switches over to start reading blocks out of the RAM A buffer, and signals to the WARP M5, via an interrupt, that B needs reloading. The WARP M5 Interrupt Service Routine (ISR) must clear this interrupt by writing to an Interrupt Acknowledge address (0xBE320074).

After buffer reload, the WARP M5 must issue a START command by writing to address 0xBE320070 to allow transmission to continue (i.e. Buffer B transmission after Buffer A is emptied).

If the empty buffer is not reloaded before the active buffer is emptied, the MSSP will stop transmitting at the end of the last valid block. The MSSP will be in a "hold" mode to allow the completion of buffer loading. The MSSP resumes transmission when it receives the START command (WARP M5 write to 0xBE320070). Note that if buffer loading lasts longer than the time to empty a buffer, the WARP M5 Interrupt Service Routine will have to handle the interrupt that is generated by the empty buffer.

To end transmission, the WARP M5 issues a STOP command (write to 0xBE32007C) when it receives the empty interrupt for the "next-to-last" buffer. This will cause the MSSP to stop all transmission after the last buffer has emptied out.

Software can monitor ongoing status by reading the BCBS Progress Register which contains the real-time block count/block size values or by reading bit 12 of the Control/Status Register. A '1' indicates that transmission is still ongoing (i.e. ATR mode is active) and a '0' indicates that transmission has stopped (i.e. switchover to LST mode has occurred).

5.4 MSSP Addresses and Registers for Control, Status and Data

The WARP M5 accesses both RAM buffers (each 32K x 16) through the same 32K set of word addresses ranging from 0xBE30.0000 to 0xBE31.FFFC (refer to Figure 6). The same range of addresses is used for both of the physical RAMs, but only A or B can be accessed at any given time. In LST mode, the WARP M5 selects which RAM will be accessed via the LOCAL_AB bit (bit 5) in the Control Register (see Table 3). In ATR mode, hardware automatically controls which buffer

is being loaded by alternating between the two RAMs. Software is simply loading data.

There are eight register addresses used to test, operate and monitor the MSSP (see Table 2). The first four are 16 bits wide and have 16-bit data associated with them. The Control/Status Register and BCBS Register provide for top-level set-up and control of the MSSP. The BCBS Progress Register can be used for real-time monitoring of the data transmission as it progresses. A spare Readback Register is used for self-test. There are four write-only addresses that are used to start and stop the data transmission process and do buffer reload handshaking. The data for these four write-only registers is "don't care".

Table 2 - MSSP Registers

Address	Function	Description	Notes
BE32.0060H	Control/Status Register	Write/Read	1. See Table 3
BE32.0064H	Block Count/Block Size (BCBS) Register	Write/Read	2. Nominal value = 0x0228
BE32.0068H	BCBS Progress Register	Write/Read	3. Write and then read
BE32.006CH	Self-Test Readback Register	Read Only	Always = 0xA5A5
BE32.0070H	Transmission START address	Write Only	4. (data = don't care)
BE32.0074H	Interrupt Acknowledge Address	Write Only	5. (data = don't care)
BE32.0078H	Not Used		
BE32.007CH	Transmission STOP address	Write Only	7. (data = don't care)

Notes:

1. All 16 bits are readable, only the 8 LSBs are writeable. See Table 3 for bit definitions.

2. Bit 15 (MSB) is a "don't care" (not used); Bits 14-10 (5 middle bits) for number of blocks in a RAM: 1 to 32 (Note all zeros is for 32); Bits 9-0 (10 LSBs) for number of half-words in a block: 1 to 1024 (Note all zeros is for 1024). The nominal value of 0x0228 will set 552 half-words per block and 32 blocks per buffer.

3. Instantaneous look at blocks already transmitted, and word (of current block) being transmitted. Write data is don't care, write strobe needed for "snapshot" of address counters.

4. Write to this address to start transmission after pre-loading the A and B RAMs with data.

5. Write to this address to clear the level-sensitive interrupt bit to the WARP M5.

6. Not used.

7. Write to this address to stop transmission at the next buffer empty occurrence.

Table 3 - Control/Status Register Bit Definitions

Bit	Meaning or Function	Bit Type
15	Reload Error Status Bit: 0 = No Error, 1 = Error	Read Only Status
14	Reload Request Bit: 0 = Reload Acknowledge, 1 = Reload Requested	Read Only Status
13	RAM being accessed by WARP M5: 0 = RAM A, 1 = RAM B	Read Only Status
12	MSSP Mode Status: 0 = LST Mode, 1 = ATR Mode	Read Only Status
11, 10	Actual Rate Selected Bit 1: 00 = 8 Mbps, 01 = 4 Mbps Actual Rate Selected Bit 0: 10 = 2 Mbps, 11 = 1 Mbps	Read Only Status Read Only Status
9	Actual Data Destination Selected: 0 or 1 = Comm RSN*	Read Only Status
8	Actual Data Source Selected: 0 = WARP M5, 1 = External MSSP	Read Only Status
7	Not defined (spare)	Write/Read Control
6	MSSP enable (when = 1)	Write/Read Control
5	Local A/B Select for LST mode: 0 = RAM A, 1 = RAM B	Write/Read Control
4	Data Bit Rate Control: 0 = Jumper Control, 1 = Software Control	Write/Read Control
3, 2	Software Rate Select Bit 1: 00 = 8 Mbps, 01 = 4 Mbps Software Rate Select Bit 0: 10 = 2 Mbps, 11 = 1 Mbps	Write/Read Control Write/Read Control
1	Software Destination Select: 0 or 1 = Comm RSN*	Write/Read Control
0	Software Data Source Select: 0 = WARP M5, 1 = External MSSP	Write/Read Control

* This allows the capability to add a second Comm RSN but for our purposes, this bit should be set to 0.

5.5 MSSP Operational Timeline

Refer to Figure 7. When the WARP M5 board is first powered on or reset, the MSSP comes up in Local Setup/Test (LST) mode. The WARP M5 "points" to the A RAM and can do write/read self tests on the A RAM and registers (via A side busses). By writing a one to Control Register (0xBE320060) bit 5, the WARP M5 "points" to the B RAM and can do write/read self tests on the B RAM and registers (via B side busses). In LST mode, the MSSP is in an inactive state (i.e. the RTS signal is deasserted and no serial clock is generated).

For data transmission, the WARP M5 sets up the MSSP by writing the Control Word to enable the MSSP (bit 6), specify destination Comm RSN (bit 1), set Comm RSN data rate, select data source (bit 0), and set Buffer B as the first buffer to load (bit 5). Once the MSSP is setup, the WARP M5 can write the Block Count/Block Size (BCBS) register (0xBE320064) (to set the number of half-words per data block (probably 552) and the number of blocks (probably 32)) and to load the

B RAM buffer. Note that the BCBS register can be written only when the WARP M5 is pointing at buffer B. The WARP M5 can load up to 32 data blocks into RAM B. Note that software has to be cognizant of the data block address boundaries if block sizes of less than 2 Kbytes are loaded (refer back to Figure 6).

Transmission starts when the WARP M5 issues the START command (write to address 0xBE320070) which switches the MSSP from the LST to the ATR mode and starts sending data blocks from RAM B. While transmission takes place, the WARP M5 writes to the RAM buffer address range which will automatically be routed to RAM A. At the end of this load, the processor re-issues the START command to continue serial transmission.

When the B RAM is empty, the MSSP changes over to start unloading from RAM A and interrupts the WARP M5 to request a RAM B reload. The WARP M5 would write to the Interrupt Acknowledge address to acknowledge (and clear) the interrupt, load the next 32 data blocks, and re-issue the START command. When the A RAM empties, the RAM switch, WARP M5 interrupt, reload, and reload acknowledge cycle would repeat.

To end transmission, the WARP M5 must issue the STOP command (0xBE32007C) after the interrupt corresponding to the next-to-last buffer. This is because the MSSP processes the STOP command (0xBE32007C) as the last buffer empties. Therefore, the minimum number of buffers that should be transmitted is two (1 each of buffer B & A) since the 1st interrupt occurs after buffer B is emptied. When the last buffer empties, the MSSP would go from ATR mode back to LST mode to indicate transmission has stopped. In order to fully terminate the MSSP, bit 6 of the Control World must be cleared to prepare the MSSP for the next download sequence. The bottom part of Figure 4 shows the buffer reload handshake and the STOP process.

Note that when clearing bit 6 of the Control Word, care must be taken not to change any of the other bits. This is because the last buffer may still be downloading. Bit 12 of the Control Word can be polled to determine the end of the last buffer (when it is a zero).

In order to estimate the time intervals required for the activities depicted in Figure 7, it is assumed that each RAM will be loaded with 32 data blocks, with each block starting at a 1 Kword address boundary, and with 552 half-words per data block. At 4 Mbps on the RF link, after Reed-Solomon encoding by the Comm RSN, each 1104-byte block will take about 2.85 msecs to transmit to the ground station. To empty 32 data blocks out of a RAM will take about (32 x

2.85 msecs) = 91 msecs. So on the average, the WARP M5 will have to reload a buffer memory every 91 msecs.

If an WARP M5 half-word read-write transfer from SSR DRAM to an MSSP buffer RAM takes about 400 nsecs, then it will take roughly (32 x 552 x 0.4 μsec) = 7066 μsecs = 7 msecs for the WARP M5 to reload a buffer (A or B) with fresh telemetry data. The processor utilization for continuous telemetry downlink would then be about 8% = 7msecs/91 msecs. This processor usage level would double for a byte-wide buffer memory, and be halved for a 32-bit wide buffer memory.

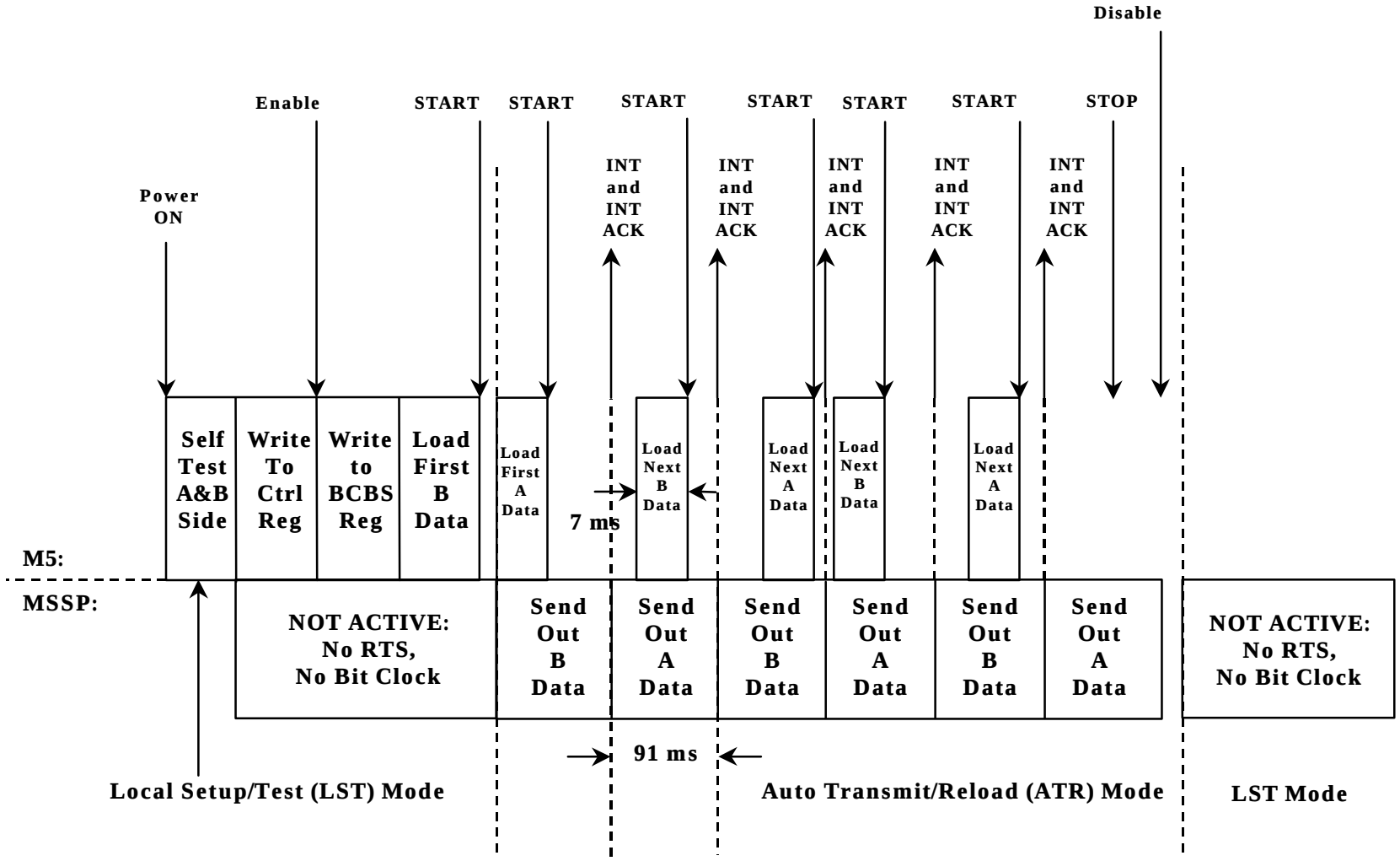


Figure 5-4- MSSP Operational Timeline